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Assessment of different Growth Techniques of Strained Germanium Heterostructures for Electronic and spintronic Devices

A.H. A. Hassan
Department of Physics, Faculty of science,
University of Tripoli.
amnahassan53@yahoo.co.uk

A. Diyaf
Department of Physics, Faculty of science,
University of Tripoli.

U. Elfurawi
Department of Physics, Faculty of science,
University of Tripoli.

A. E. Abubkr
Department of Physics, Faculty of science,
University of Tripoli.

Abstract

This paper, emphasis different growth techniques of two-dimensional hole gas of strained germanium (sGe) heterostructure, molecular beam epitaxy (MBE) and chemical vapor deposition (CVD). sGe heterostructure has become an important material as a replacement material to Silicon in P-type devices because of its higher hole mobility and lower effective mass. Researchers study this material in terms of electrical and spintronic devices according to technology demands for devices with higher efficiency and low power consumption. High hole mobility up to $1 \times 10^{6}\mathrm{cm}^{2}/\mathrm{Vs}$ at temperature of 1.5 K has been reported for normal structure declaring high quality samples with low density dislocation and low interface roughness.

These samples were grown using Reduced Pressure Chemical Vapour Deposition (RP-CVD) indicating high purity system and the affordability of this technique in terms of electronic and spintronic devices.

Keywords Strained Germanium, MBE, CVD, High purity system.

1. Introduction

Although the first transistor was made of germanium (Ge), silicon (Si) is the main component in device fabrication mainly due to the good quality of the interface of Si with its natural oxide (SiO_2), and it is abundant compared to Ge therefore cheaper. On the other hand, Ge does not possess a good interface with its natural dielectric, GeO_2. Nevertheless, Ge is again considered as a significant candidate for future Metal-Oxide-Semiconductor Field Effect Transistor (MOSFETs), as it has a higher bulk mobility being more than 4 times that of Si for holes and 2 times for electrons as seen in Table 1.

Gordon Moore in 1965[1] has observed that the number of transistors on an integrated circuit doubles approximately every couple of years, an observation that become known as Moore's Law. This remarkable feature has been achieved through a phenomenon known as scaling a systematic reduction of the MOSFET dimensions. Which, in turn has been attained by advancements in device fabrication techniques and, the advancements in lithographic techniques that helps in decreasing dimensions to be determined [1].

The continued performance enhancements in Complimentary Metal-Oxide-Semiconductor (CMOS) circuits cannot be achieved by scaling alone. Indeed, a major concern is the cost of new fabrication plants. However, of even greater importance could be that MOSFET dimensions are rapidly approaching a regime where the key device features consist of just a few hundred atoms. In this regime quantum effects such as tunneling become significantly problematic, resulting in higher leakage currents and power consumption. There are many materials with intrinsically superior electrical properties compared to silicon, which have found roles in the market applications such as optical devices and the high frequency components of mobile communication devices. One of the most promising materials is Germanium (Ge).

Strained Si technology has been extensively used to improve the performance of advanced Si integrated circuit recently. However, due to the strong demand of high drive current to increase circuit speed, Si has reached its limit especially in p-type MOSFET. For that reason, sGe becomes a promising alternative to Si CMOS devices. Introducing strain to Ge leads to the effective mass reduction and mobility enhancement. The strain also splits the heavy_light hole bands further reducing the (100) in plane effective mass and the interband scattering as well [2]. High dielectric constant materials should be applied between the gate and the substrate such as SiO_2 and HfO_2 in terms of minimising the power consumption of MOSFETs that accounted for gate current leakage [1]. Germanium has emerged as a good alternative to silicon in terms of p-type MOSFETs because it comes from the same IV group as Si, but with a smaller bandgap (0.67eV) and significantly higher hole mobility as shown in Table (1).

High hole mobility devices required a good hole confinement in Ge layer, since the latter grown directly on Si is just thermally stable below 1nm thickness, which is not suitable for device application. Introducing SiGe layer virtual substrate (VS) on Si helps to increase the thickness of Ge layer and improves the hole confinement. This paper aims to introduce some of a significant research area in modulation doped strained Ge heterostructures in terms of improving the quality of the structure by employing different growth techniques, and investigating their effect on structural characterization such as channel thickness, strain and scattering mechanism of the carriers in Ge quantum well.

Table 1: Si, Ge and GaAs selected property comparison at 300K

	Si	**Ge**	**GaAs**
Mobility(cm^2/Vs)	μ_e=1500 μ_h=450	μ_e=3900 μ_h=1900	μ_e=8500 μ_h=340
Lattice constant (A^o)	5.431	5.646	5.653
Energy Gap (eV)	1.12	0.67	1.42
Intrinsic carrier concentration (cm^3)	1.0×10^{10}	2.0×10^{13}	2.1×10^{6}

2. Discussion

The key growth technique for Heterostructures including strained Germanium quantum well is Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD). Regarding to the requirement of high mobility devices that raise their speed and performance, scientists attempt to acquire high quality material with few defects. Different efforts have been made to investigate the most effective growth technique to give low treading dislocation density, low surface roughness and the highest mobility. There are two main ways of epitaxial growth:

The main characteristic of the MBE growth technique [3, 4] is that it has independent control of growth parameters, low controllable growth temperatures enabling minimisation of solid state out diffusion and auto doping, also the low growth rates and shutter control permits thin, highly uniform layers to be grown. Whilst solid source MBE (SS-MBE) has demonstrated high wafer uniformity and ultra-sharp doping profiles, the method does have some limitations. A major limitation is the lack of in-line calibration is particularly missed during the growth of thick (several microns) epilayers and arises from the depletion of the solid-source material. Typically, for the growth of SiGe epilayers, the solid atomic sources are evaporated via electron beam impingement. However, as the sources are consumed material flux calibrations are required on a rather frequent basis which is time consuming. SS-MBE is therefore quite a slow growth process and is mainly reserved for research rather than industry.

CVD procces offers high growth rates, simultaneous growth of wafers, and it is more stable and reproducible for thick structures, a gas containing the material wished to be deposited, known as a "precursor", is passed over a heated substrate [5]. Under the correct conditions the gas will chemically react with the substrate and deposit epilayers. The standard chemical gases used for the SiGe system are silane and germane, which are passed down a furnace tube using a carrier gas, typically hydrogen. In addition, the growth of thick layers is possible since the gas sources are effectively infinite and the gas ratios can be constantly maintained and monitored throughout the growth via the use of mass flow control units. It is therefore the technique favoured by industry, and the major different between these two Technique are summarized in Table 2.

Table 2: The major different between CVD and MBE growth technique

CVD	MBE
Pressure around 0.5-760 torr	Requires UHV with Pressure below 10^{-8} torr
High growth rate	Low growth rate (1 atomic layer or less at a time) = high uniform layers
Useful for experiments and mass production	Useful for research lab experiments

Growth technique is the main responsible parameters to get an optimal characterisation in the samples, that affects the purity of the channel, the defects like surface and interface roughness, threading dislocation density (TDD)and the accuracy of the layers thicknesses. These parameters reflects on the electrical characterisation such as carrier mobility and sheet density, as well as, the optical properties. The transport properties of the two dimensional hole gas in sGe quantum well (QW) have been the focus of intensive research for many years because of its potential for device applications. Both low temperature (LT) [5, 6-10] and room temperature (RT) [11-19] measurements have been performed in order to obtain a better understanding of the fundamental physics behind these transport properties.

To obtain an improved electrical performance for sGe, a high purity Ge QW needs to be grown on a Ge-rich buffer layer with a low defect density. Hole mobilities at RT of up to 3000 cm^2 /V s [10, 12, 15, 17, 19] have been reported for structures grown via Low Energy Plasma

Enhanced Chemical Vapour Deposition (LEPE-CVD) [19, 20] and SS-MBE [13, 17]. However, growth by the Reduced Pressure Chemical Vapour Deposition (RP-CVD) utilizing a low growth temperature methodology has enabled a pure sGe QW (Si concentration less than 0.01 at.%) [11] to be grown, leading to the highest reported hole mobility to date for sGe at 10 K (1.1 × 10^6 cm^2 /V s at a sheet density of 3 × 10^{11} cm^{-2} [6], while at the room temperature (RT) mobility extracted using a simulation methods helps to analysis the data and defined the mobility and sheet density of the channel excluding the carriers in the parallel channels. Mobility of (3.9 ± 0.4) × 10^3 cm^2 /V s was determined by maximum entropy-mobility spectrum analysis (ME-MSA) for a sheet density (p_s) 9.8 × 10^{10} cm^{-2}, and by using another method for mobility simulation (Bryan's Algorithm Mobility Spectrum (BAMS)) mobility of (3.9 ± 0.2) × 10^3 cm^2 /V s for a sheet density (p_s) 5.9 × 10^{10} cm^{-2} has extracted which confirmed the high RT mobility for this structure [21]. More higher mobility at RT of 4230 cm^2 /V s for a sheet density (p_s) 1 × 10^{11} cm^{-2} has determined using the ME-MSA technique by Myronove et al [22]. These results were the highest mobility reported for mobility at room temperature as seen in Figure 1.

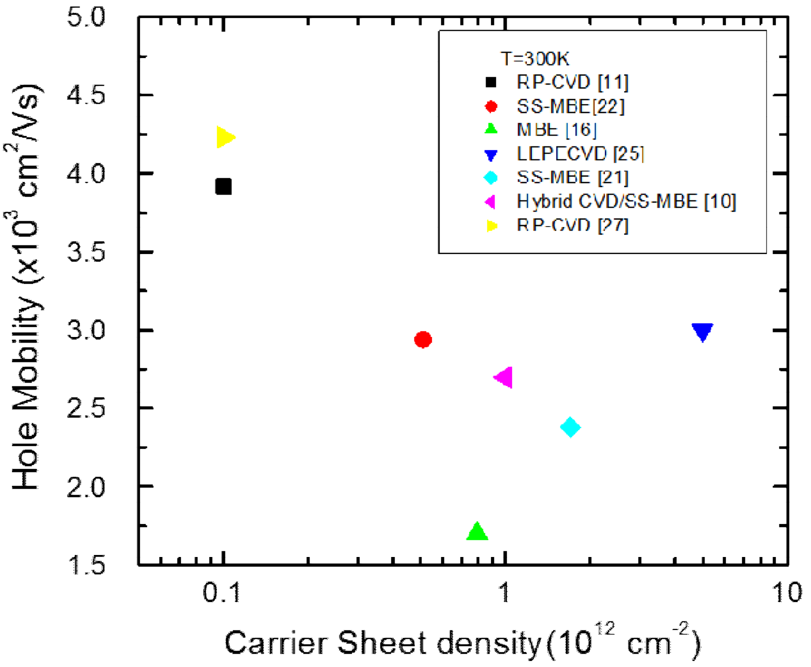

Figure 1: Room temperature hole mobility of strained germanium devices grown by different growth technique.

(LEPE-CVD) [5] which is considered as a good choice for a high growth rate 10 nm/s. Strained germanium modulation doped structure result in a high hole mobility of 1.2×10^5 cm^2 /Vs at temperature of 2 K with a sheet density of 8.5×10^{11} cm^{-2}, which was thought to be due to the high quality structure, with low interface roughness compared to other techniques[5]. By optimizing this method (LEPE-CVD) for appropriately chosen plasma densities and substrate temperatures, abrupt interfaces can be achieved on both sides of the Ge channels. Additional hydrogen is supplied to the reactive gases, even for channel widths above the critical thickness for dislocation formation and it ended with high mobility 9×10^4 cm^2 /Vs at sheet density 6×10^{11} cm^{-2} at 4.2 K[38]. It has been seen that LT processing below 600°C is essential for high performance devices to avoid Si-Ge interdiffusion at high temperature at the Ge/SiGe interface. Annealing at temperatures above 600°C causes a reduction in mobility and an increase in the sheet density of the structure under study. Moreover, Ge layers beyond the critical thickness easily relax when the annealing temperature is increased above 500°C.

Surface roughness is an important parameter to get high mobility samples and for the inverted structure it has more effect on the top of the channel, for this reason increasing the thickness will drop its effect which separate the roughness from the carriers that located near the bottom of the channel [23]. Introducing two steps LT buffers account for no significant different between the mobility of normal and inverted structure, which shows mobility at low temperature of $1.4\times10^{4}\mathrm{cm}^{2}/\mathrm{Vs}$ and $1.3\times10^{4}\mathrm{cm}^{2}/\mathrm{Vs}$ respectively [4] owing to the smooth surface compared with Ge structure on graded buffer layers. in terms of enhance mobility(higher than 3000 cm^{2}/Vs at room temperature) and reduce surface roughness for samples fabricated by LEPECVD, they suggest more optimisation for the growth temperature [18]. Another kind of CVD growth mechanism, used by Myronov et al [21], is (RP-CVD) with a reverse linearly graded buffer, which improves the root mean square (rms) surface roughness to about 1.5 nm with TDD of 2×10^{6} cm^{-2} . This is comparable to that achieved by LEPE-CVD with a thinner virtual substrate (VS) (3µm to reach 80% Ge), in comparison to the VS grown by LEPE-CVD (above 10µm to reach 80% Ge).

Symmetric doping modify the Ge QW valance band energy from triangular like to rectangular like that increase mobility of room and low temperature by 3.3 and 1.7 times its previous values, respectively as reported by Myronov et al [15]. However, in another study symmetric doping produces two subband energy in quantum well that increase the interband scattering which drastically reduce the hole mobility [8]. The mobility of two dimensional hole gas (2DHG) for sGe channel has been studied heavily by researchers [6, 9, 11, 13, 18, 24-27]. However, the significant enhancement in mobility of sGe channel has reported by Dobbie et al [6] using RP-CVD, and in the same time the highest mobility for two dimensional electron gas in sSi was revealed to be $(1.6-2)\times 10^{6}\mathrm{cm}^{2}/\mathrm{Vs}$ [28] as shown in Figure 2.

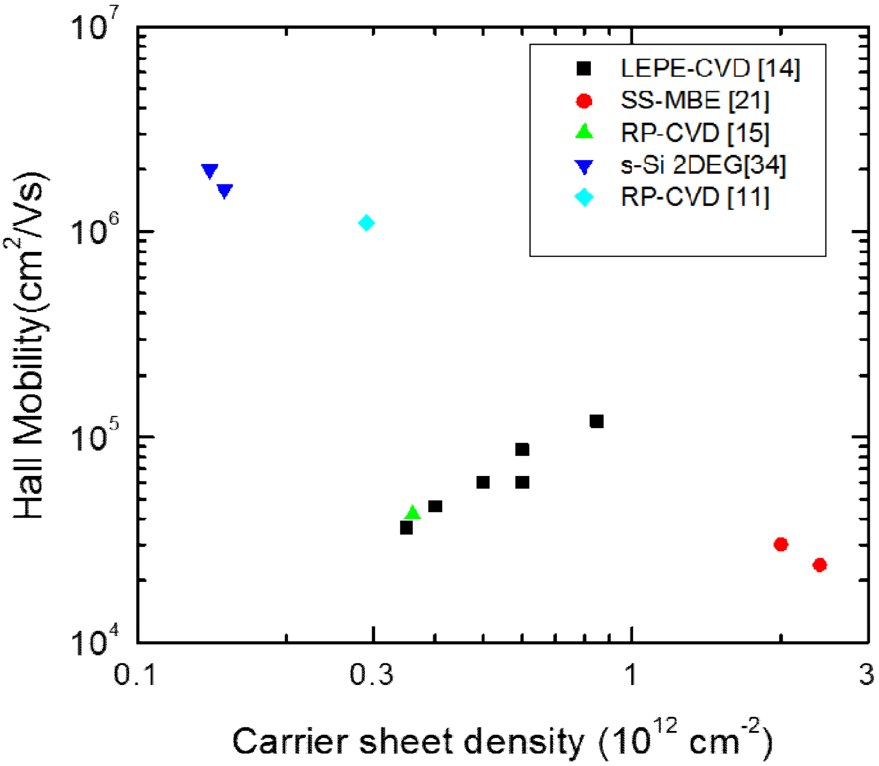

Figure 2: Low temperature hole mobility of strained germanium devices grown by different growth technique.

These high mobilities open a new field of characterisation for 2DHG in sGe such as fractional quantum Hall effect and spin splitting effect properties. The investigation of Rashba spin splitting in 2DHG of sGe materials has opened the door of using these materials in spintronic devices [30-33] . The zero field spin splitting raises from bulk or structural inversion asymmetry (BIA and SIA respectively), BIA is excluded in Ge because of its crystal symmetry and only SIA has been observed in sGe samples (Figure 3) in low magnetic field of magnetoresistance [29]. The fractional quantum Hall effect has also been investigated in high magnetic field and showed optimistic result for devices with high mobility [34], The different growth techniques show also significant mobility anisotropy in different growth orientations that explains the mobility different in the same sample with different orientation [35].

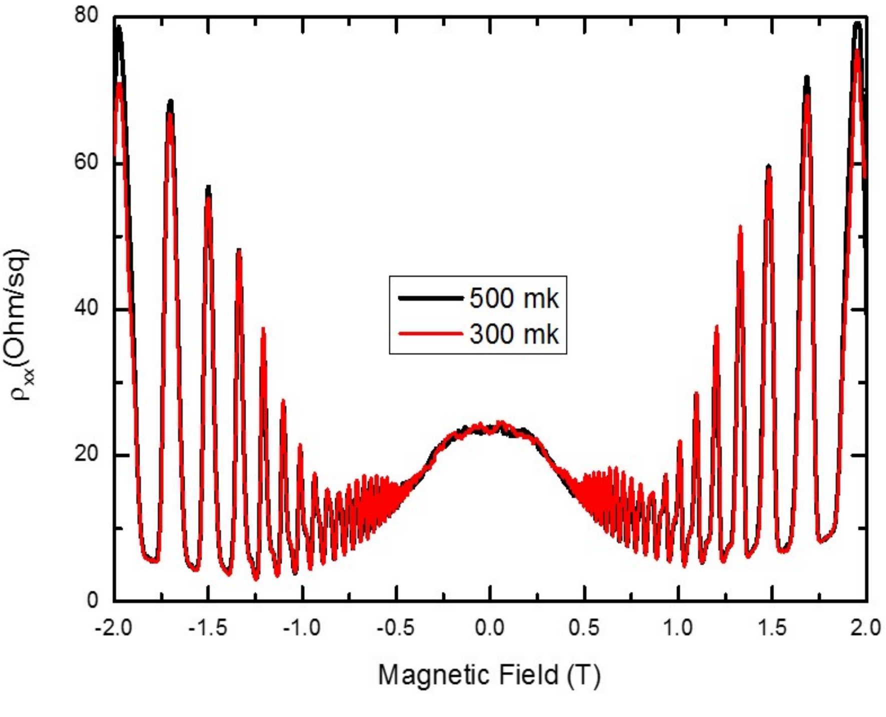

Fig 3. magnetoresistance as a function of magnetic field for sGe channel sample shows Rashba spin splitting for both temperatures 300 mK and 500 mK.

Li et al [36] attempts to get high quality samples using MBE, which investigated a low temperature technique (LT-MBE) for $Si_{0.7}Ge_{0.3}$ on Si (001) and found that using this process gives a lower (TDD) in the order of 10^5 cm^{-2} for a smaller overall layer thickness and smother surface. This development in the quality of the structure was an excellent motivation for Ueno et al [4, 37] who applied a low temperature buffer ($Si_{0.3}Ge_{0.7}$) for p-type sGe channel to examine the effect of this method on the properties of a Ge channel. Two paths were followed to grewthe sample; one and two step LT techniques and employing SS-MBE. They found that the two step LT buffer produced a single period of surface roughness with a 10 nm amplitude whereas the one step LT technique produced many periods. The one step process Leads to a higher drop of mobility, whilst the two step LT buffer generated a high mobility at room temperature (1700 cm^2 /Vs) because of the low TDD (1×10^5 cm^{-2}), small surface roughness (1-3 nm), and almost total relaxation (>95%).

Sawano et al found out that sheet density enhancement with temperature depend on the growth technique of SiGe buffer carrier [7]. Structures grown by LT buffer has a higher increase in sheet density than the structure grown with graded SiGe buffer at higher temperature, in other words, the effect of conduction layer is higher for LT SiGe buffer. Also they found that GS-MBE is better for fabricating SiGe layer, because SS-MBE generate an accepter like point defect which is a source of parallel conduction, furthermore, these defects is a significant reason for current leakage in MOS devices.

The effect of Ge channel thickness on SiGe (VS) has been studied by Irisawa et al[13] where they reported that the optimised channel thickness is 7.5 nm for high mobility strained germanium channel on $Si_{0.3}Ge_{0.7}$. Reducing the channel thickness less than that will drop the mobility dramatically, owing to the boost of the effect of surface roughness, whereas increasing channel thickness, reduces the mobility because of strain relaxation[23]. Nevertheless, strain relaxation on graded SiGe buffer could be controlled using LT technique with chemical mechanical polishing (CMP). This structure experiences a good improvement in mobility by reducing the effect of interface roughness. Therefore, more reduction in channel thickness does not influence the mobility [38,40,41].

To enhance the performance of the structure in terms of reduced doping, Ge segregation, and reduced surface roughness, researchers have also attempted to apply a combination of two growth methods such as LEPE-CVD and SS-MBE techniques [39]. This resulted in a large increase in room temperature mobility, 2700 cm^2 /Vs at sheet density $1x10^{12}$ cm^{-2}, as well as a significant improvement in the conductance that is important for device applications.

3. Conclusion

In summary, different growth techniques have been discussed for 2DHG sGe heterostructure and important different in the structures properties are reviewed. It has been shown that RP-CVD technique produces a high purity sample with low treading dislocations and low interface roughness, which result in high mobility reached of $1 \times 10^6 \mathrm{cm}^2/\mathrm{Vs}$ at sheet density of 3×10^{11} cm^{-2} at low temperature which states clean and pure system of growth with very low contamination allows for new feature that make sGe as an important material in the field of electronic and spintronicdevices.

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